14. (new) The system of claim 5, wherein subsets of audio data are stored in one of the memory banks and stored audio data is read from a second of the memory banks.

15. (new) The system as set forth in claim 5, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.

REMARKS

This Amendment is in response to the Office Action mailed May 14, 1999. In the Office Action, claims 1-9 are rejected under 35 U.S.C. §112, second paragraph. Claims 1-8 are rejected under U.S.C. §102(e) and claim 9 is rejected under 35 U.S.C. §103(a). The abstract is objected to. Applicant has amended Claims 1, 3, and 5, and added Claims 10-15 without introducing new matter. The abstract is also amended. Reconsideration in light of the amendment and remarks made herein is respectfully requested.

The abstract was objected to. The abstract has been amended to address the issues raised. Therefore, the objection should be withdrawn.

In the Office Action, claims 1-9 are rejected under 35 U.S.C. §112, second paragraph. In particular, the Examiner stated the "N" and "P" are indefinite. In response, Applicants have amended Claims 1 and 5 to remove references to "N" and "P".

Claims 1-8 are rejected under 35 U.S.C. §102(e) and claim 9 is rejected under 35 U.S.C. §103(a) in view of Vizireanu. Although the office action applies the grounds for rejection together to all the claims, applicants would like to address the independent claims separately.

With respect to claim 1, Vizireanu neither teaches nor discloses "providing a second plurality of memory banks, each memory bank being accessible to the first and second processors". The office action cites elements 340 as teaching first and second processors. However, elements 340 are audio servers which are part of computer 320. Therefore, Vizireanu appears to have only one processor, that is computer 320. There is no teaching or disclosure that the servers are processors as set forth in the claims. In fact elements 340 appear to be functioning as audio output ports for the computer 320.

Furthermore, each server is coupled to a particular VCR. There is no teaching or disclosure, assuming arguendo that the elements 340 are processors, that each memory bank is accessible to the first and second processor, as set forth in claim 1. Furthermore, there is no teaching or disclosure that access is for operations selected from the group comprising read and write operations.

In addition, Vizireanu neither teaches nor discloses storing subsets of said audio data in the second plurality of memory banks, said subsets corresponding to different groups of audio. Vizireanu's VCRs are not memory banks. Real time audio access, for example, read and write operations, is not possible using VCRs; there is simply no teaching or disclosure by Vizireanu of the claimed present invention. To the contrary, in Vizireanu, audio is recorded on the VCRs for purposes of overdubbing on particular video tapes.

Thus, for the reasons noted above, independent claim 1 as well as dependent claims 2-4 are distinguished over the Vizireanu reference.

Claim 5 is also distinguished over the Vizireanu reference. Vizireanu neither teaches nor discloses a first processor and a second processor coupled to said first and second busses. The office action notes that Vizireanu disclosues "first and second busses 365" (page 3, 5/14/99 office action). However, element 365 is actually described as control coupled coupled between each VTR control card 360 and a respective VTR unit. The office action further provides that elements 340 are the "processors". Elements 340 are not coupled to lines 365. Thus, as set forth in the claims, there is no teaching or disclosure of the first and second busses coupled to the first processor and second processor.

In addition, Vizireanu neither teaches nor discloses second plurality of memory banks coupled to said first and second buses for storing said audio data, said second plurality of memory banks being accessible to the first and second processors for operations selected from the group comprising read and write operations, said second plurality of memory banks storing subsets of audio data, said subsets corresponding to different groups of audio channels.

Therefore, independent claim 5, as well as dependent claims 6-9 are distinguishable over the Vizireanu reference.

New claims 10-15 are also distinguished over the Vizireanu reference for the reasons noted above. In addition, claims 10 and 11 are further distinguishable, as Vizireanu does not teach or disclose storing subsets of data in an interleaving manner. Claims 12 and 14 are further distinguished over Vizireanu as Vizireanu neither teaches nor discloses storing one of the subsets of audio data in one of the memory banks and reading stored audio data from a second of the memory banks. Claims 13 and 15 are further distinguished as Vizireanu does not teach or disclose the first processor performing a read

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operation on a first memory bank and the second processor performing a write operation on a second memory bank.

In summary, claims 1-15 are distinguished over the cited art and are in condition for allowance. Allowance of the claims is respectfully requested.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,
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Dated: September 1, 1999

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on ~~August 26, 1999~~ 9/1/99 cc

C Clinkenbeard September 1, 1999
Cheri Clinkenbeard Date

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